

A Thermally-Actuated Bistable MEMS Relay

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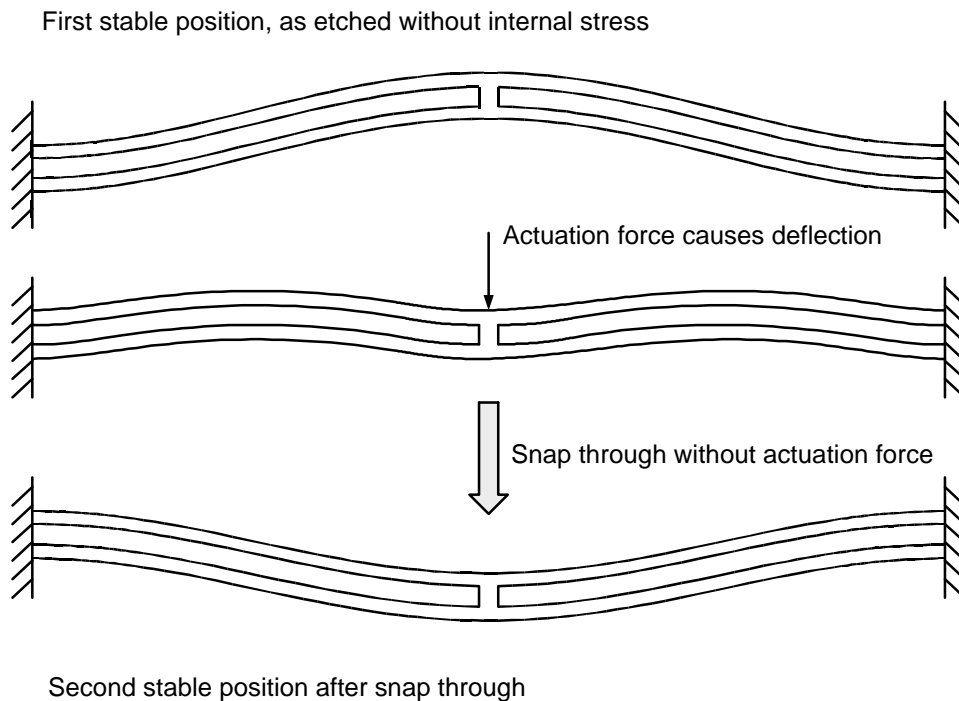
MIT MTL Student Review

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Contents

- **Components Design**
Bistable Structure. Thermal Bender. Relay Contact.
- **Process Development**
Shadow wafer. DRIE structure metalization. Anti-footing. Fracture stress enhancement.
- **Prototype Relay**
Design, fabrication and test.

Bistable structure design



- **Double-Beam geometry:**

Initial apex height d_0 , thickness t , length L , width (normal to paper) b .
Moment of inertial $I = b \cdot t^3 / 12$

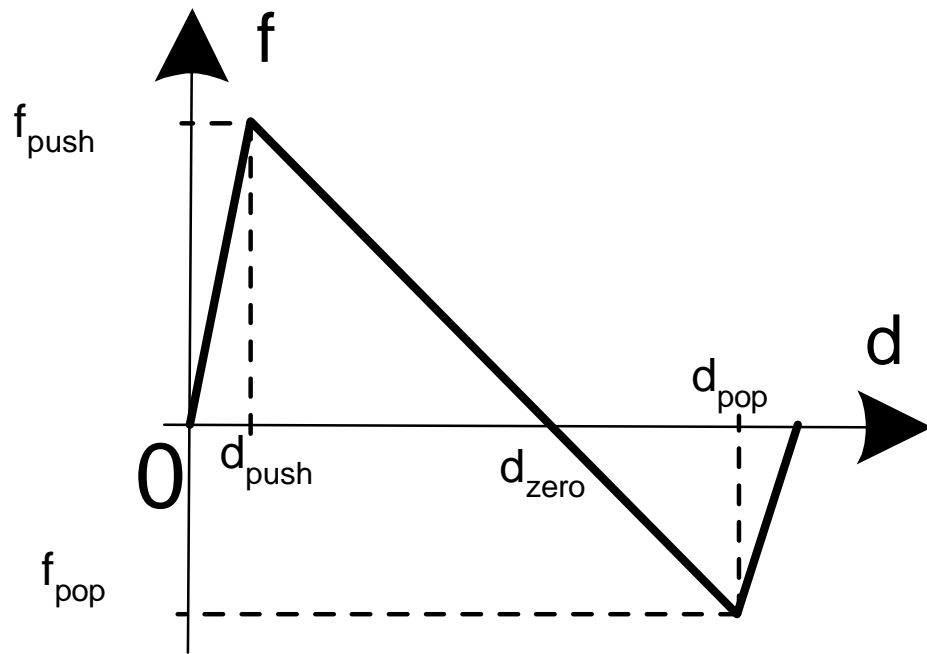
- **Modeling:**

Force-displacement ($f-d$) of the beam center determined by the beam buckling mode analysis.

- **Key parameter:**
 $Q = d_0 / t$

When $Q > 2.35$, structure is bistable;
when $Q > 6$, $f-d$ characteristics asymptotes to a closed form.

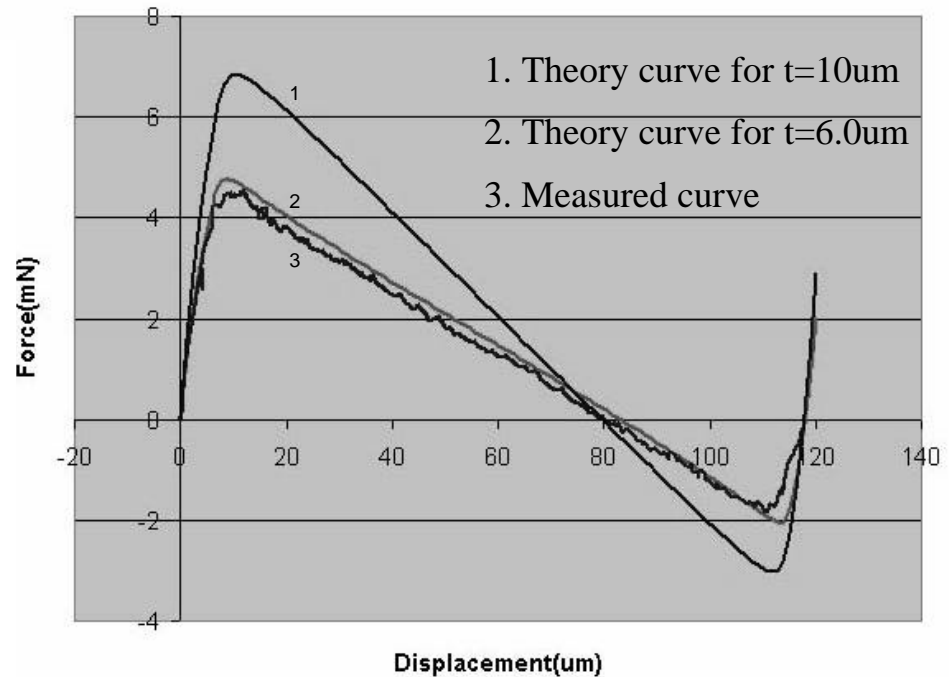
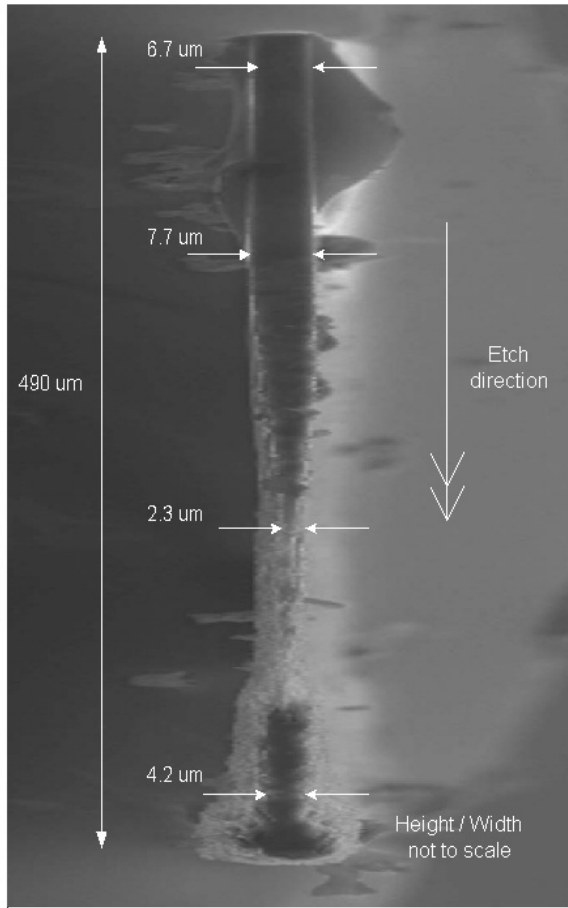
Double-beam f-d curve



With $Q(=d_0/t) > 6$

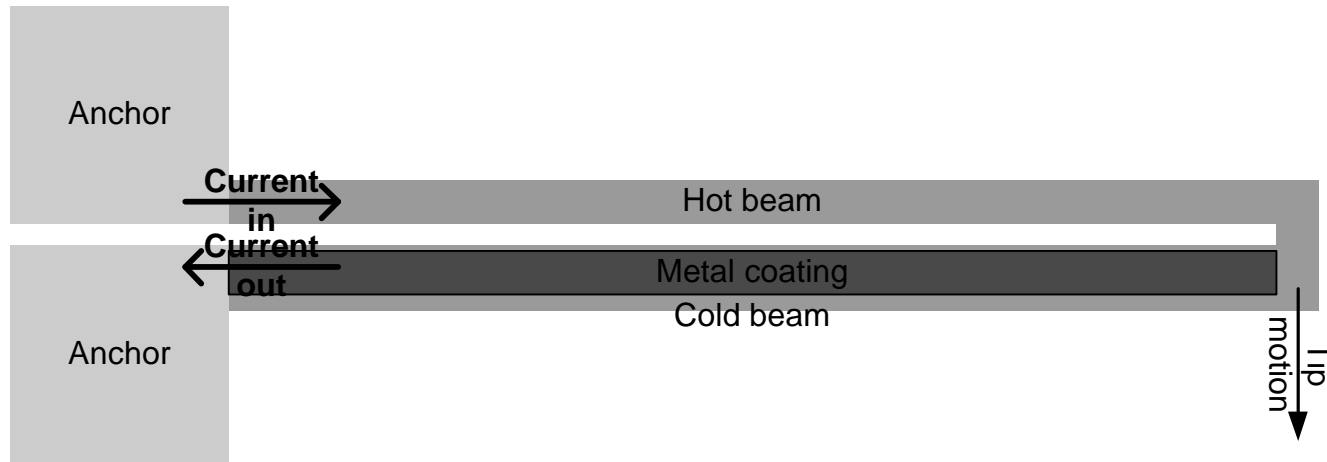
- $f_{\text{push}} = 1516 E I d_0 / L^3$
- $d_{\text{push}} = 0.03 d_0$
- $d_{\text{zero}} = 1.33 d_0$
- $f_{\text{pop}} = 768 E I d_0 / L^3$
- $d_{\text{pop}} = 1.99 d_0$
- Max strain $\epsilon_{\text{max}} = 2450\% t d_0 / L^2$

Double-beam fab. and test



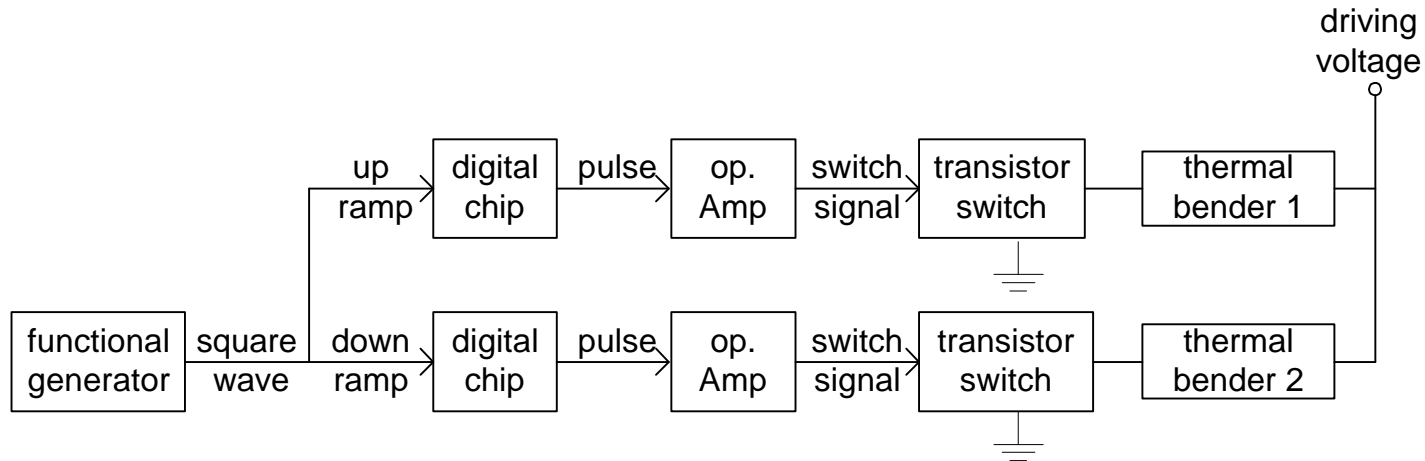
- DRIE through etch a 490 μm wafer.
- Thickness variation along the etch direction
- Average $t=6\mu\text{m}$, smaller than mask value 10 μm .
- Measurement agrees very well with the theory

Thermal bender design and modeling



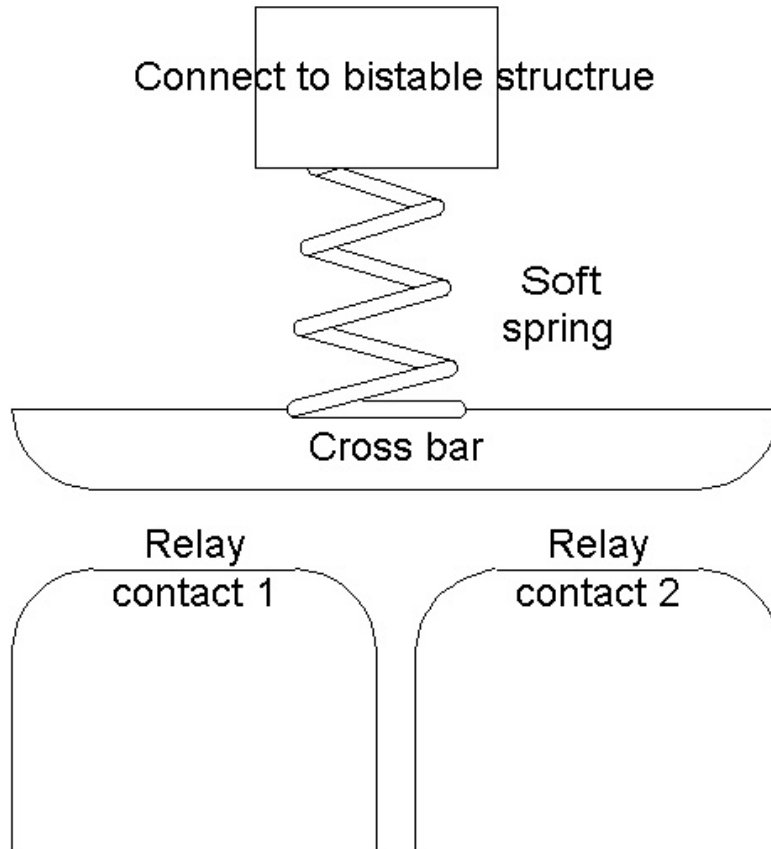
- **Mechanical modeling:** Nonlinear equations for two axially-loaded beam connected at the tip solved numerically.
- **Mechanical efficiency:** If the hot beam is thin, upward buckling of the hot beam would significantly lower the expansion difference. So we avoid the thin hot beam design.
- **Joel heating differential:** Induced by coated metal.
- **Thermal efficiency:** Temperature difference would be very low after reaching thermal equilibrium, so we design the actuator to be a thermally transient one.

Thermal bender driving circuit



- One bender to push the bistable structure down, the other to push it up.
- Timing controlled by the up and down ramps of the square wave.
- The pulse width controlled by R and C in the digital chip circuit.
- The amplitude of the actuation pulse controlled by the driving voltage.

Relay contact design



- Flat-flat contact to ensure maximum contact area.
- Spring coupling balances the force on two contacts. And with compliance in the paper depth, it helps two taper shaped surface contact better.
- The gap between crossbar and contacts determined by soft spring stiffness and bistable structure characteristics.

Process development

- Shadow wafer bonding as a metalization mask.
- Cleaning/edge-rounding process for better metalization on sidewalls of DRIE etched structures.
- Anti-footing process for good relay contact.
- Techniques to enhance the effective fracture stress of DRIE structures.

Shadow wafer as hard mask

- A through-etched shadow wafer could be temporally bonded to the device wafer by following the fusion bonding procedures but without the annealing step.
- Shadow wafer could be easily separated in water after Au metalization.
- But with high temperature process, e.g. tungsten(high melting point) e-beam, the bond is hard to separate.

Processes matrix study for metalization

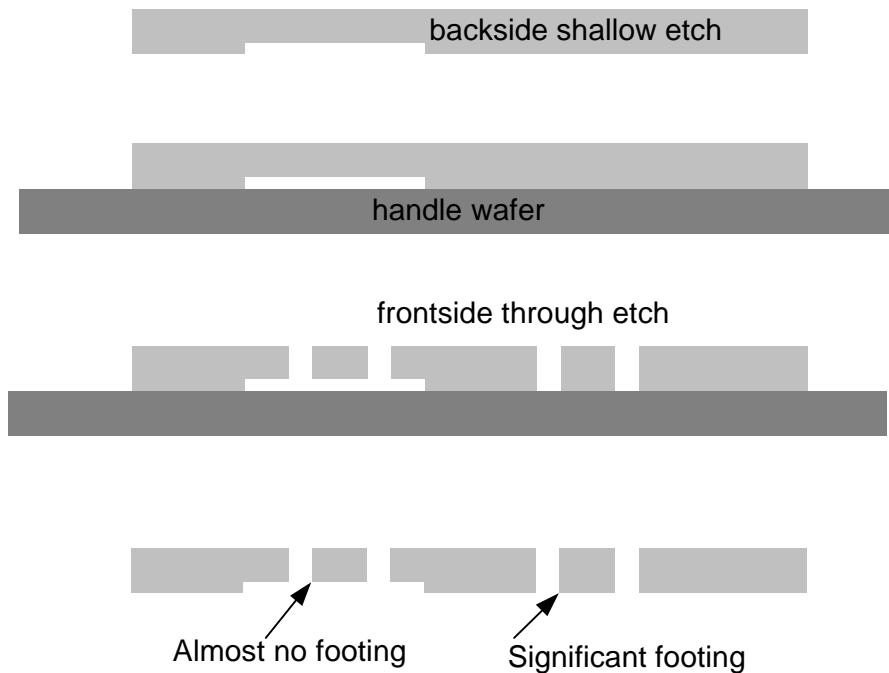
1. 100um deep channels are etched by DRIE,
2. SF6 etch and Asher O2 plasma for cleaning the Teflon from the DRIE,
3. Oxidation for further cleaning and for rounding off the edge between the wafer surface and its sidewall,
4. HF for removing the oxide and further rounding off the edge,
5. Angled e-beam and sputtering for coating the metal,
6. wafer die sawed in a designed way to control the current path in two resistance measurements,
 - Full channel test current path: wafer surface – sidewall – channel bottom – sidewall – wafer surface,
 - Half channel test current path: wafer surface – sidewall – wafer surface.
7. The measured R indicates the metalization quality.

Metalization processes matrix and R measurement

Wafer piece #	sts MIT69A 90mins	sts SF614 20secs	Asher O2 30secs	Thermal SiO2 30mins	HF etch the oxide	Sputter Au(0.9um)	Angled ebeam Au 0.54um	Full channel (Ohm)	Half channel (Ohm)	Adhesion
	DA11	yes	yes	yes	yes	yes	yes	0.026	0.21	
	DA21	yes	yes	yes	yes		yes	0.129	0.31	
	DB11	yes	yes	yes			yes	0.226	0.29	some peel
	SA21	yes	yes		yes		yes	0.069	0.44	some peel
	SA11	yes	yes		yes	yes	yes	0.097	N/A	peel off
	SB11	yes	yes				yes	0.353	N/A	peel off
	SB12	yes	yes				yes	N/A	N/A	
	DB12	yes	yes	yes			yes	N/A	2.7	
	DA12	yes	yes	yes	yes	yes	yes	N/A	15.7	
	DA22	yes	yes	yes	yes		yes	N/A	34.9	
	SA12	yes	yes		yes	yes	yes	N/A	43.5	some peel
	SA22	yes	yes		yes		yes	N/A	51.7	

Best: sputtering with all cleaning/edge-rounding steps.

Anti-footing techniques



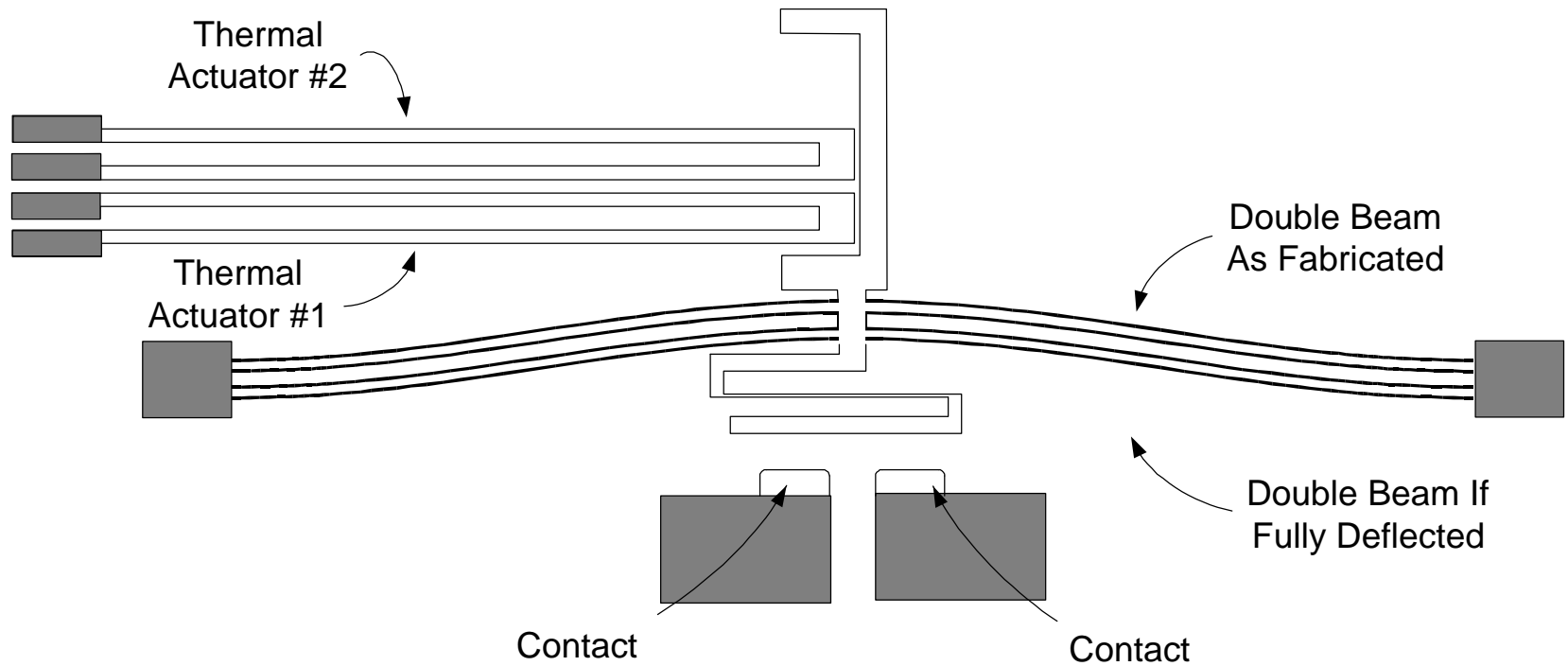
- Footing effect
 1. Weak etch power resulting in incomplete etch at the bottom
 2. Reflected ion erodes silicon
- Bad for
 1. Relay contact: the wide bottom structure makes point contact.
 2. Stress concentration.
- The backside recess etch (~20um) effectively alleviates the footing problem.

Fracture strain enhancement

- Effective fracture strain(EFS) is determined by material and process.
- EFS affects the reliability of device and is a key design constraint. The bistable double-beam's size is determined by the EFS by $L = m^2 * 37.6 / (\epsilon_{\text{eff}}^2) * E b * Q * f_{\text{pop}}$
- Thermal Oxidation increases EFS by smoothing the sharp edge from DRIE and footing. The EFL would be lowed with the BOE removal of oxide, but it is still higher than before the oxidation.
- The transparency mask has a zigzag shape along the edge of features, it has lower EFS than with the real mask.
- The anti-footing technique also would increase EFS by much, data to be collected.

	Real mask, DRIE, SF6 etch 20sec	Cheap mask, DRIE, SF6 etch 20sec	Left + thermal SiO2 0.5 um	left + BOE	With anti- footing tech.
EFS	0.18%	0.1%	0.2%	0.15%	TBD
f_{pop} / L $Q=6,$ $b=300\text{um}$	1.2mN/mm	0.38mN/mm	1.5mN/mm	0.88mN/mm	TBD

Plan view of the relay



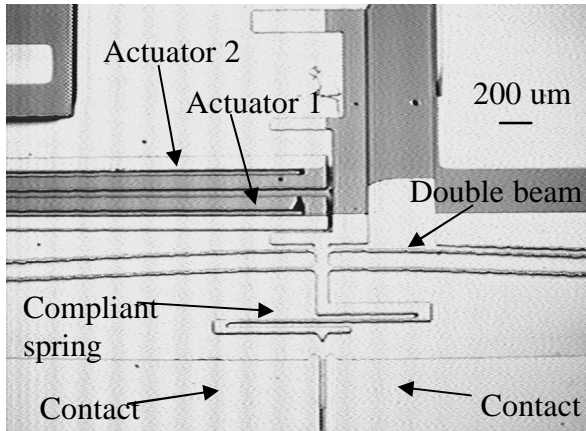
A prototype relay with transparency mask

- Transparency mask is used, with minimum feature size $\sim 20\mu\text{m}$, the relay is designed bigger than it would be with a real mask.
- Low receptivity $\sim 0.01\text{ohm}\cdot\text{cm}$ wafer is selected for: lower thermal bender actuation voltage; little diode effect with probe.
- $300\mu\text{m}$ thick wafer is used to save DRIE time and also ensures that $10\mu\text{m}$ thick resist is a thick enough mask.
- Double-beam size: 8mm long, $20\mu\text{m}$ thick, $120\mu\text{m}$ apex height. It can apply 2mN on each contact.
- Thermal bender size: 1.2cm , $125\mu\text{m}$ thick, $50\mu\text{m}$ gap. With 200K degree temperature, it has maximum force of 15mN , stroke of $200\mu\text{m}$.
- All device feature is drawn on mask with a halo gap of $50\mu\text{m}$.

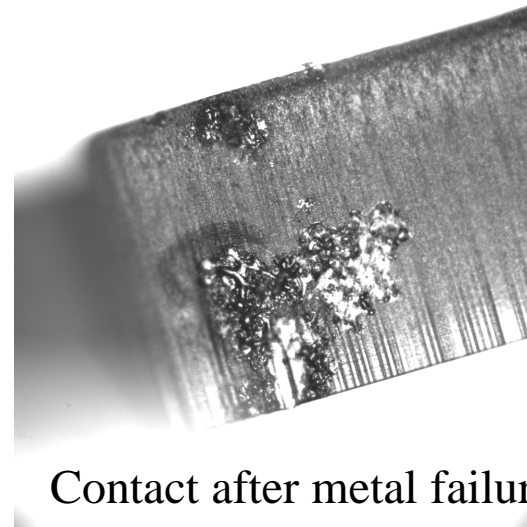
Main fabrication steps

- Handle wafer: e-beam coat Ti and Cr double side, etch pit ~100um by HF.
- Device wafer: backside recess etch, front side through etch, grow 0.5um thermal oxide, AME5000 remove the top oxide.
- Shadow wafer: Through etch, as a hard mask for metalization.
- Bonding: anodic bonding, bond shadow wafer with device wafer without annealing.
- Sputtering 1um Au, separate the shadow wafer from device.

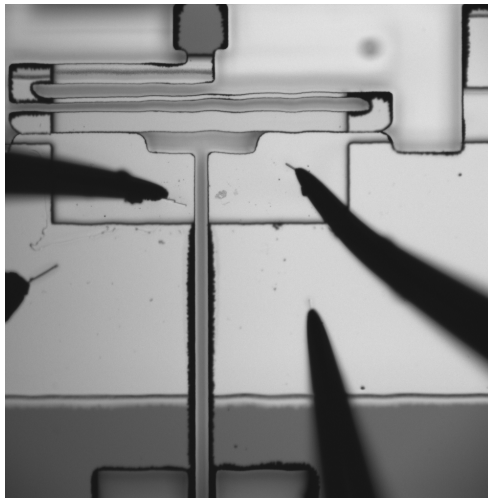
Some pictures of the prototype relay



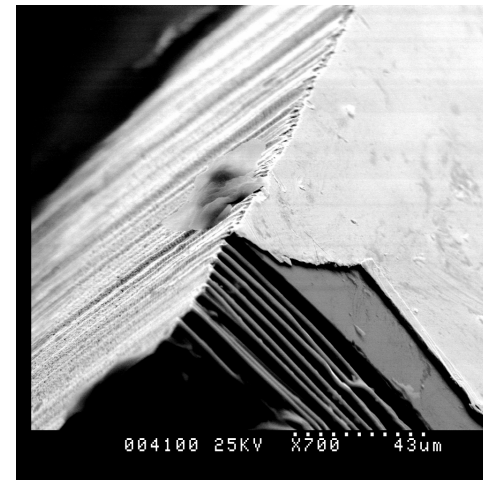
Main components



Contact after metal failure



Relay is on



Metalization

Test results of the prototype relay

- On resistance $\sim 0.3\text{ohm}$.
- R doesn't decrease with more contact force applied manually.
- Cold switching max current, $\sim 1.5\text{A}$.
- Hot switching 100mA for several cycles, before metal fails.
- Cycle test 100,000 times, when metal on thermal bender fails(evaporated).
- Max voltage when off: $>200\text{V}$.

Future work

- More process and design improvement to achieve better contact resistance and lifetime etc, e.g. an annealing step after metalization to ensure good adhesion.
- Use stepper to have 10:1 size reduction transparency mask. This will decrease the mask waviness a lot, and increase EFS and contact quality.
- Develop packaging process.
- Finally use the real mask to build a compact relay with super functional specs.